ACHARYA INSTITUTE OF TECHNOLOGY
Bangalore - 560090

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10EE766

Seventh Semester B.E. Degree Examination, Dec.2016/Jan.2017
Electromagnetic Compatibility

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer FIVE full questions, selecting at least TWO questions from each part.***
2. ***Missing data if any may be suitably assumed.***

PART – A

1 a. Explain, with an example, the various interferences that can occur in an equipment and hence explain the importance of EMC. **(06 Marks)**

b. Explain what is meant by designing for EMC. **(06 Marks)**

c. Explain part-15, subpart-J of FCC regulation. Also list the radiation and conduction emission limits for Class A and Class B devices. **(08 Marks)**

2 a. Derive an expression for noise voltage induced in conductor 2 in a system of 2 base conductors. Conductor 1 is having a source of V_1 volts at ω rad/sec frequency. Discuss the variation of noise voltage with frequency. **(06 Marks)**

b. Consider two conductors 1 and 2. Conductor 1 has a source and 2 has a shield which is grounded. A part of the conductor extends beyond the shield. Derive an expression for the noise voltage induced in conductor 2. Discuss the effect of conductor extending beyond shield. **(08 Marks)**

c. Stray capacitance between conductors 1 and 2 is 50 pF. Each conductor has a capacitance to ground of 150 pF conductor 1 has 10 V ac signal at 100 kHz on it. What is the noise voltage picked up by conductor 2 if it is terminated (i) in infinite resistance (ii) in 1000 Ω resistance (iii) in 50 Ω resistance. Comment on the results. **(06 Marks)**

3 a. Obtain an expression for the noise voltage due to magnetic. Coupling between open wire and a shielded cable with the shield grounded at both the ends. Plot the noise voltage versus frequency and show the shielding effectiveness on the plot. **(06 Marks)**

b. Explain how protection against magnetic field at the receptor can be achieved by decreasing the receptor loop area. Hence show that only limited magnetic field shielding to possible in a circuit grounded at both the ends. **(08 Marks)**

c. Derive an expression for the mutual inductance between coplanar loops as shown in Fig. Q3 (c). **(06 Marks)**

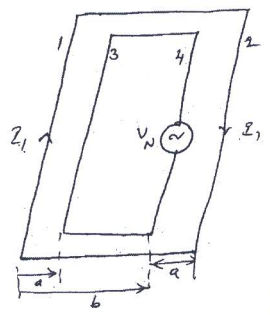

Fig. Q3 (c)

4 a. Explain how ground loops become a source of noise. Also explain the various methods of eliminating or minimizing them. **(06 Marks)**

b. Derive an expression for the noise voltage in a circuit with common mode choke and at low frequency. Also plot $\frac{V_N}{V_G}$ versus frequency. **(08 Marks)**

4 c. Fig. Q4 (c) shows the equivalent circuit of a differential amplifier circuit where $V_G = 100mV$, $R_G = 0.01\ \Omega$, $R_S = 500\Omega$, $R_{C_1} = R_{C_2} = 1\ \Omega$, $R_{L_1} = R_{L_2} = 10K\Omega$. Obtain the noise voltage at the terminals of the amplifier. If $RL_1 = RL_2 = 100K\Omega$. What is the noise voltage and discuss the results. **(06 Marks)**

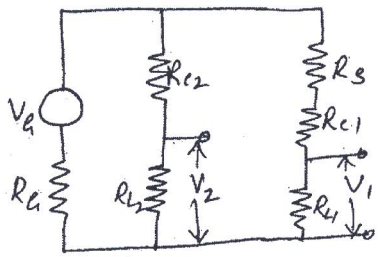

Fig. Q4 (c)

PART – B

5 a. Discuss the role played by balancing in reducing / eliminating the noise pick up. **(06 Marks)**

b. Explain the power supply decoupling. Also discuss how impedance of the power distribution system affects the noise pick up and how it can be reduced. **(06 Marks)**

c. Discuss the following:
(i) Emitter follower circuit driving capacitive load.
(ii) High frequency filtering.
(iii) System band width.
(iv) Modulation and coding **(08 Marks)**

6 a. Discuss the following:
(i) Reflection loss due to plane wave.
(ii) Reflection loss in near field. **(08 Marks)**

b. Discuss the electric and magnetic field losses in the far field. **(06 Marks)**

c. Explain the effect of multiple reflections in thin shield. **(06 Marks)**

7 a. Explain the following:
(i) Shielding with magnetic materials.
(ii) Apertures.
(iii) Seams. **(06 Marks)**

b. Write briefly on: (i) Conductive gaskets and (ii) Conductive coating. **(08 Marks)**

c. What is the reflection loss of 0.001 in thick copper shield to a 1000 Hz electric field? If the thickness is increased to 0.01 in what is the reflection loss? **(06 Marks)**

8 a. Explain ESD mechanism with examples. How these discharges becomes hazard to electronic equipments. **(04 Marks)**

b. Explain the following with respect to ESD:
(i) Insulated enclosures.
(ii) Keyboards and control panels.
(iii) Circuit design and board layout. **(08 Marks)**

c. Explain the following software error detecting techniques:
(i) Errors in program flow.
(ii) Input-output errors.
(iii) Data memory errors. **(08 Marks)**

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